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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/631,098
Filing Date: July 31, 2003
Appellant(s): VOLDMAN, STEVEN H.

Frederick W. Gibb, III
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 4/14/06 appealing from the Office action mailed on 11/16/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,242,763	Chen et al.	06-2001
6,015,992	Chatterjee et al.	01-2000
5,631,793	Ker et al.	05-1997

5,528,188	Au et al.	06-1996
5,314841	Brady	05-1994
5,039,873	Sasaki	08-1991

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14, 17, 18 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al. (USP 5,528,188) in view of Brady et al. (USP 5,314,841).

With respect to claims 14 and 17, Figure 4b of the Au et al. reference discloses a device which includes: a MOSFET transistor (Q1) comprising a gate (gate of Q1), a body (body of Q1); an RC discriminator circuit (32) comprising a resistor (R) and a capacitor (C), and a circuit control network (40) modulating a potential of the body (of M) to provide ESD protection (the circuit of 40 capable of controlling the potential biasing the body of the transistor and therefore it also capable of provide ESD protection) . The Au et al. reference does not disclose that the MOSFET Q1 in Figure 4b is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15). Therefore, it would have

been obvious to one having an ordinary skill in the art at the time the invention was made to modify the circuit in Figure 4b of the Au et al. reference by using specific SOI technology to fabricate the MOSFET transistor for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claims 14 and 17. Note that, in this modification, "the body that is floating with respect to an underlying substrate" on line 3 of claim 14 is met when fabricate the device by using SOI technology (i.e., the body of Q1, Figure 4b in the above modification is floating with respect to an underlying substrate) because the body of an SOI MOSFET is floating with respect to an underlying substrate. Also, note that, the functional limitation in claim 17 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage.

With respect to claims 31 and 32, the modification/combination of Au et al. and Brady et al. as discussed in claim 14 above meets all the limitations of this claim except that the resistor R is a resistive-transistor. However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that the circuit is easily fully

integrated. With such a modification, the limitation of claim 31 is met as that the RC discriminator including a resistive-transistor and a capacitor (also note that because the circuitry is fabricated by using SOI technology as discussed in claim 14, so the body of the SOI transistor is floating with respect to an underlying substrate). Note that, in the above modification, the functional limitation in claim 32 is also met as the operation of control network circuitry modulates the potential voltage of the body and limit the body to a reference voltage. Also, note that the device includes a source S and a drain D (Figure 4b of Au et al.), wherein the source is connected to the resistive-transistor (both connected to ground), and the drain is connected to the capacitor as recited in claim 34; and the functional limitation that the resistive transistor and said capacitor initiate coupling of the gate when an over-voltage or over-current condition exits (recited in claim 35) is also met (Col. 5, lines 30-67 of Au et al.) and also because the structure of the RC discriminator connected to the gate of the MOSFET device of the Au et al. is substantially identical as the structure of the RC discriminator of the inventions. Also, Figure 4b of the Au et al. shows a PAD (PAD) coupled to the capacitor (for claim 36).

With respect to claims 18 and 33, the modification/combination as discussed in claim 31 meets the limitations of these claims that the circuit control network (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology (discussed in claim 14), and because every resistor in the circuitry is formed by using an always ON MOSFET transistor (as discussed in claim 31) so the SOI MOSFET in this claim is the always ON MOSFET transistors for resistors R1 and R2 in circuit 40 of Figure 4b.

3. Claims 24 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188), and further in view of Brady et al. (USP 5,314,841).

With respect to claim 24, Figure 2 of the Ker et al. reference discloses a device which includes: an n-channel MOSFET (Mn1) comprising a first body and a first gate; a p-channel MOSFET (Mp1) comprising a second body and a second age; a first RC discriminator (Rn, Cn1) comprising a first resistor (Rn) and a first capacitor (Cn1); and a second RC discriminator (Rp , Cp1) comprising a second resistor (Rp) and a second capacitor (Cp1). The Ker et al. reference does not discloses the device a first circuit control network for modulating a potential voltage of the first body, and a second circuit control network for modulating a potential voltage of the second body. However, the Au et al. reference discloses in Figure 6 a device that includes first and second circuit control networks (SCR 52 and 50, wherein the detail of the SCR is shown as circuit 40 in Figure 4b) for controlling the first and second bodies (bodies of Q3 and Q2), respectively for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event (see line 59 of Col. 5 to line 23 of Col. 6). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to provide the device of Figure 2 of the Ker et al. reference with the first and second circuit control networks connected to the first and second bodies, respectively, for the purpose of improving the level of ESD protection of either a positive or negative polarity ESD event. Thus, this modification meets the limitations of the first and second circuit control networks as recited in claim 24 including the functional limitation "to provide ESD protection".

The combination of the Ker et al. reference and the Au et al. reference meets all the limitations of claim 24 except that the circuitry is fabricated by using silicon-over-insulator SOI technology. However, the Brady et al. reference discloses that silicon-over-insulator (SOI) technology provides advantages over regular silicon technology such as increasing the operating speed and reducing the power consumption of the circuitry (Col. 1, lines 12-15 of Brady et al.). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify above combination by using specific SOI technology to fabricate the circuitry for the purpose of increasing the operating speed and reducing the power consumption of the circuitry. Thus, this modification meets all the limitation of claim 24. Note that, in this modification, "a fist body that is floating with respect to an underlying substrate" on line 3-4 and "a second body that is floating with respect to said underlying substrate" on line 6-7 of claim 14 is met when fabricate the device by using SOI technology (i.e., the bodies of Mp1 and Mn1, Figure 2 of Ker et al. in the modification are floating with respect to the underlying substrate) because the body of an SOI MOSFET is floating with respect to an underlying substrate

With respect to claim 26, Figure 2 of the Ker et al. in the above combination shows the n-channel SOI MOSFET Mn1 comprises a source and a drain connected to the first resistor (Rn) and the first capacitor (Cn1); and the p-channel SOI MOSFET transistor includes a source and a drain connected to the second resistor (Rp) and the second capacitor (Cp1).

With respect to claim 27, the functional limitation that the first resistor and capacitor and the second resistor and capacitor initiate coupling of the first gate and the second gate, respectively, when an over-voltage or over-current condition exists is met (see line 65 of Col. 4

to line 5 of Col. 5). Further, because the structure of the first and second RC discriminator circuit connected to the first and second gates is substantially identical to applicant's invention so it must functions the same.

With respect to claim 28, it is seen in the operation of the combination/modification circuitry that the first circuit control network limits the first body to a reference voltage, and the second circuit control network limits the second body to the reference voltage (both of the circuit control networks SCR in the above combination/modification are the same so they must limit the same reference voltage).

With respect to claim 29, it is seen that the two circuit control networks SCR in the above combination/modification coupled to difference voltages, i.e., the one that is coupled to the body of the p-channel MOSFET is coupled to the power supply voltage, and the one that is coupled to the body of the n-channel MOSFET is coupled to ground.

With respect to claim 30, the above combination/modification circuitry shows a pad (21, Figure 2 of Ker et al.) connected between the n-channel and p-channel SOI MOSFETs.

4. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (USP 5,631,793) in view of Au et al. (USP 5,528,188) and Brady et al. (USP 5,314,841).

With respect to claim 25, the modification/combination of Ker et al., Au et al. and Brady et al. as discussed in claim 24 above meets all the limitations of this claim except that first and second circuit control network comprises at least one SOI MOSFET. However, it is art-recognized that a resistor could be easily implemented in an integrated circuitry by using a transistor that has its gate connected to DC bias so that the transistor is in an ON state (evidence is shown in the Sasaki reference, USP 5,039,873, that a MOSFET transistor is functionally

equivalent to a resistor when the MOSFET transistor is ON, see Figure 4c, and Col. 1, lines 21-22 of Sasaki). Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the above combination/modification circuitry by substitute an always ON MOSFET transistor (i.e., a MOSFET transistor having a DC bias at its gate so that the MOSFET transistor is ON) for each of the resistors in the circuitry because they are functionally equivalent and for the purpose that it is easily integrated. With this modification, the limitations of this claim is met because the first and second circuit control networks (40, Figure 4b of Au et al.) includes at least a SOI MOSFET because the circuitry is fabricate by using SOI technology, and because every resistor in the circuitry is formed by using an always ON MOSFET transistor so the SOI MOSFET in this claim is the always ON MOSFET transistors (for resistors R1 and R2 in circuit 40 of Figure 4b of Au et al.).

(10) Response to Argument

With respect to the combination of the Au reference and the Brady reference, Appellants argue that the Au reference does not disclose using the claimed "control circuit network" in a floating (silicon-over-insulator) structure. However, this argument is not persuasive because the rejections were not made under 35 U.S.C. 102. Instead, the rejections were made under 35 U.S.C. 103.

Appellants further argue that the combination of Au and Brady destroys the operability of the Au reference because the circuit in Au cannot be fabricated using SOI technology since an SCR (silicon controlled rectifier) cannot be fabricated using SOI technology. However, this argument is not persuasive because, as the Examiner indicated in the Advisory Office Action mailed on 1/27/06, it is capable of fabricated an SCR by using SOI technology (evidence is

shown in U.S. Patent 6,242,763 (see lines 8-11 of Col. 1, and lines 61-67 of Col. 2) issued to Chen et al. on June 5, 2001, and in U.S. Patent 6,015,992 (see abstract, and line 56-64 of Col. 7) issued to Chatterjee et al. on Jan 18, 2000). Thus, an SCR is capable of operating when fabricated in SOI technology, and thus the circuit in Au is capable of fully operating when fabricated in SOI technology.

Appellants further argue that if the device in Au were transferred to the SOI technology field, this would destroy the operability of the device in Au because Au relies on the body being non-floating, and non-SOI structures do not insulated the body from the underlying substrate, while in SOI structure the body is insulated (floating). However, this argument is not persuasive because, when modified the circuit of Au by fabricated the circuit in SOI environments, the body of transistor Q1in Figure 4b of Au is still being controlled by the network 40 which is similar as applicant's invention that the body of the transistor is also controlled by a body controlled network. Note that, when fabricated in SOI technology, the circuit would have the advantages of low power and high speed.

Appellants further ague that because it is improper to modify the Au reference (as shown above) there is no teaching of such features defined by independent claims 1 and 31. However, this argument is not persuasive because it is proper to fabricated the circuitry of the Au reference using SOI technology as suggested by the prior art that an SCR is capable of operating when fabricated in SOI technology (again, evidence is shown in U.S. Patent 6,242,763 (see lines 8-11 of Col. 1, and lines 61-67 of Col. 2) issued to Chen et al. on June 5, 2001, and in U.S. Patent 6,015,992 (see abstract, and line 56-64 of Col. 7) issued to Chatterjee et al. on Jan 18, 2000), it

would have been obvious for the skilled artisan to employ such technology to produce a high speed circuit with lower power requirement.

With respect to dependent claims 17, 18 and 32-36, appellants argues that Au cannot transfer to an SOI environment, so the combined teachings of Au and Brady would not teach or suggested to one skill in the art the features that are defined by dependent claims 17, 18 and 32-36. However, this argument is not persuasive for the same reasons discussed above. The proposed modified of the Au reference to be fabricated using SOI technology is suggested by the prior art (again, evidence is shown in U.S. Patent 6,242,763 (see lines 8-11 of Col. 1, and lines 61-67 of Col. 2) issued to Chen et al. on June 5, 2001, and in U.S. Patent 6,015,992 (see abstract, and line 56-64 of Col. 7) issued to Chatterjee et al. on Jan 18, 2000).

With respect to the combination of the Ker et al. reference, the Au reference and the Brady reference, Appellants argue that the Au reference does not disclose using the claimed "control circuit network" in a floating (silicon-over-insulator) structure. However, this argument is not persuasive because the rejections were not made under 35 U.S.C. 102. Instead, the rejections were made under 35 U.S.C. 103.

Appellants, again, argue that Au would not operate in a silicon-over-insulator (SOI) structure since an SCR (silicon controlled rectifier) cannot be fabricated using SOI technology. However, this argument is not persuasive because, as the Examiner indicated in the Advisory Office Action mailed on 1/27/06, an SCR is capable of being fabricated using SOI technology (evidence is shown in U.S. Patent 6,242,763 (see lines 8-11 of Col. 1, and lines 61-67 of Col. 2) issued to Chen et al. on June 5, 2001, and in U.S. Patent 6,015,992 (see abstract, and line 56-64 of Col. 7) issued to Chatterjee et al. on Jan 18, 2000). Thus, an SCR fabricated in SOI

technology will operate properly as shown by the prior art, and the circuit in Au is capable of fully operating when fabricated in SOI technology.

Applicants further argue that if the devices in Au and Ker were transferred to the SOI technology field, this would destroy the operability of the devices in Au and Ker because Au and Ker rely on the body being non-floating, and non-SOI structures do not insulated the body from the underlying substrate, while in SOI structure the body is insulated (floating). However, this argument is not persuasive because, when modified the circuits of Ker and Au by fabricated the circuits in SOI environments, the body of each transistor in the modification/combination of Ker and Au is controlled by a body control network, and when the MOSFET transistors are fabricated using SOI technology, the body of each transistor is still controlled by a respective body control network which is also similar as appellants' invention that each body of the respective transistor is also controlled by a respective body controlled network. Note that, circuits fabricated in SOI technology have the advantages of low power and high speed.

Appellants further argue that because it is improper to modify the Au reference (as shown above) there is no teaching of such features defined by independent claim 24. However, this argument is not persuasive because it is proper to modify the Au reference as discussed above, so the combination/modification of Ker, Au and Brady meets all the limitations of claim 24.

With respect to dependent claim 25, applicant argues that Sasaki uses RC network which is connected to a pad, a resistor, a capacitor and this is electrically connected to the gate of a MOSFET between the pad and ground potential; thus, Sasaki teaches gate modulation and not body modulation. However, this argument is not persuasive because, as discussed in the rejection of claim 25, the Sasaki reference is used as an evidence that an ON MOSFET transistor functions

as a resistor so that it is obvious to one skill in the art use a MOSFET transistor that has its gate connected to a DC bias so that the transistor is always ON to implement a resistor for the purpose of easily integrated and the circuitry is being fully integrated. Note that because the circuit is fabricated using SOI technology, so the MOSFET transistor that is used to implement the resistor is also an SOI MOSFET transistor.

With respect to dependent claims 26-30, appellants argues that Au and Ker are not properly combined with Brady as shown above, so the combined teachings of Ker, Au and Brady would not teach or suggested to one skill in the art the features that are defined by dependent claims 26-30. However, this argument is not persuasive because it is proper to modify the Ker and Au references by fabricated the circuitry using SOI technology as discussed above that an SCR is capable of operating when fabricated in SOI technology (again, evidence is shown in U.S. Patent 6,242,763 (see lines 8-11 of Col. 1, and lines 61-67 of Col. 2) issued to Chen et al. on June 5, 2001, and in U.S. Patent 6,015,992 (see abstract, and line 56-64 of Col. 7) issued to Chatterjee et al. on Jan 18, 2000).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Timothy Callahan, SPE

Darren Schuberg, SPE

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PRIMARY EXAMINER